Abstract

A test structure and a test method for determining misalignment occurring in integrated circuit manufacturing processes are provided. The test structure includes a first conductive layer having a first testing structure and a second testing structure, a dielectric layer thereon, and a second conductive layer on the dielectric layer. The second conductive layer includes a third testing structure and a fourth testing structure, which respectively overlap a portion of the first testing structure and the second testing structure in a first direction and a second direction. The first direction is opposite to the second direction. The method includes a step of measuring the electrical characteristic between the first and the second conductive layers to calculate an offset amount caused by the misalignment.